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**Rancang Bangun Modul Praktikum ADC Sigma-Delta Orde Pertama Berbasis Komponen Fungsional Terpisah
sebagai Media Pembelajaran**
Aurrydiena Angelica Venantia, Enas Dhuhri Kusuma, S.T., M.Eng.;Ir. Prapto Nugroho, S.T., M.Eng., D.Eng., IPM.
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INTISARI

Pemahaman mengenai prinsip *oversampling* dan *noise shaping* pada ADC sigma-delta sering kali bersifat abstrak karena ADC sigma-delta komersial umumnya diimplementasikan dalam bentuk *integrated circuit* (IC) yang bersifat *black-box*, sehingga proses internal modulator sulit diamati dan dipelajari secara langsung. Penelitian ini bertujuan untuk merancang dan merealisasikan modul ajar sigma-delta ADC orde pertama yang disusun dari komponen aktif fungsional terpisah (komponen diskret) sebagai media pembelajaran, sehingga setiap blok fungsional penyusun modulator dapat diamati dan diukur secara langsung.

Modulator direalisasikan menggunakan op-amp TL072 (sebagai *summing amplifier* sekaligus integrator dan DAC 1-bit), komparator LM311, dan D *flip-flop* 74HC74. *Bit stream Pulse Density Modulation* (PDM) keluaran modulator diakuisisi menggunakan mikrokontroler STM32F401CCU6 Blackpill melalui antarmuka SPI *slave* dengan DMA sirkular, kemudian diolah menjadi data *Pulse Code Modulation* (PCM) menggunakan empat algoritma *decimation filter* (*Simple Downsampling* + IIR, SINC^3, SINC^3 + kompensasi FIR, dan FIR *Direct-Form*) yang diimplementasikan pada perangkat lunak berbasis Python. Kinerja sistem dievaluasi menggunakan metrik RMSE, MAE, SNR, THD, SINAD, ENOB, dan kemiringan *noise shaping* dengan ADC internal STM32 sebagai pembanding.

Hasil pengujian menunjukkan bahwa keempat algoritma *decimation* menghasilkan kualitas rekonstruksi yang relatif setara, sehingga SINC^3 dipilih sebagai algoritma utama berdasarkan keseimbangan kualitas dan kompleksitas komputasi. Pada kondisi nominal ($f_s = 400$ kHz, $f_{in} = 100$ Hz), sigma-delta ADC mencapai SNR 43.3 dB dan ENOB 6.25 bit, dengan kinerja terbaik pada $f_s = 600$ kHz (SNR 47.7 dB, ENOB 6.30 bit), melampaui ADC internal STM32. Mekanisme *noise shaping* terbukti bekerja melalui nilai kemiringan positif ($+16.8$ dB/dec pada $f_s = 400$ kHz) dan peningkatan SNR seiring kenaikan OSR. Batas operasi sistem teridentifikasi pada frekuensi *clock* maksimum 2200–2300 kHz dan *dynamic range* sebesar 7.18 dB.

Penelitian ini menyimpulkan bahwa modul praktikum yang dikembangkan berhasil mendemonstrasikan prinsip kerja sigma-delta ADC secara langsung dan terukur. Selain itu, modul ini dapat mempermudah proses pengamatan mekanisme *oversampling*, *noise shaping*, dan pengaruh ketidakidealan komponen analog nyata.

Kata kunci : modulator sigma-delta, *noise shaping*, *decimation filter*, media pembelajaran, STM32

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ABSTRACT

The oversampling and noise shaping that govern a sigma-delta ADC are often hard to understand and observe, because commercial converters are packaged as integrated circuits whose internal stages behave as a black box and cannot be probed or measured directly. To address this, the present work designs and builds a first-order sigma-delta modulator from separate functional active components and assembles it into a hands-on laboratory module, so that each functional block of the modulator can be observed and measured directly during operation.

The modulator was constructed around a TL072 op-amp, which serves as the summing amplifier, integrator, and 1-bit DAC, together with an LM311 comparator and a 74HC74 D flip-flop. An STM32F401CCU6 Blackpill microcontroller captures the modulator's Pulse Density Modulation (PDM) bit stream through an SPI slave interface backed by circular DMA. The captured bit stream is then converted into Pulse Code Modulation (PCM) data by four decimation filter algorithms implemented in Python, namely simple downsampling with an IIR filter, SINC^3, SINC^3 with FIR compensation, and a direct-form FIR. System performance was assessed using RMSE, MAE, SNR, THD, SINAD, ENOB, and the measured noise shaping slope, with the STM32 internal ADC taken as a reference.

The four decimation algorithms produced comparable reconstruction quality, so SINC^3 was adopted as the primary algorithm for its balance between accuracy and computational cost. At the nominal setting ($f_s = 400$ kHz, $f_{in} = 100$ Hz), the sigma-delta ADC reached an SNR of 43.3 dB and an ENOB of 6.25 bits, with the best result obtained at $f_s = 600$ kHz (47.7 dB and 6.30 bits), both exceeding the internal STM32 ADC. The noise shaping mechanism was confirmed by a consistently positive slope ($+16.8$ dB/dec at $f_s = 400$ kHz) and by an SNR that rose as the oversampling ratio increased. The system's operating limits were found to be a maximum clock frequency between 2200 and 2300 kHz and a dynamic range of 7.18 dB.

These results show that the developed module successfully demonstrates the working principles of a sigma-delta ADC in a direct and quantifiable manner. As a learning medium, it makes oversampling, noise shaping, and the effects of real analog component imperfections directly observable, aspects that remain hidden in IC-based implementations.

Keywords : sigma-delta modulator, noise shaping, decimation filter, learning module, STM32