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Implementasi Filter Digital IIR Butterworth Orde Empat Berbasis Biquad Cascade pada FPGA Basys3
Adji Pangestu, Ir. Agus Bejo, S.T., M.Eng., D.Eng., IPM.; Dzuhri Radityo Utomo, S.T, M.E., Ph.D
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DAFTAR PUSTAKA

[1] B. A. Shenoi, *Introduction to Digital Signal Processing and Filter Design*. John Wiley & Sons, 2006.

[2] Digilent Inc., *Basys 3 FPGA Board Reference Manual*, 2016, revision April 8, 2016, DOC# 502-183.

[3] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, 3rd ed. Pearson, 2010.

[4] Xilinx Inc., "Infinite impulse response filter structures in xilinx FPGAs," 2009, xilinx White Paper WP330.

[5] E. Pinheiro, O. Postolache, and P. Girão, "Fixed-point implementation of infinite impulse response filters," *Metrology and Measurement Systems*, vol. 17, no. 2, pp. 217–232, 2010.

[6] O. Zoubek and T. Musil, "High performance IIR filter FPGA implementation utilizing SOS microcode core," *Transactions on Electrical Engineering*, vol. 8, no. 2, pp. 22–25, 2019.

[7] A. Jayaswal, A. Rathore, H. Choudhary, and S. Kumar, "Design and hardware realization of a dynamically adjustable IIR filter on FPGA for real-time noise monitoring and suppression," in *Intelligent, Sustainable, Social, and Secure Computing*, 2025, pp. 118–125.

[8] Z. Qiang, S. Jing, W. Weilian, Y. Ruping, and C. Cheng, "Design of fourth-order IIR digital filter based on FPGA," in *International Conference on Electronic Measurement Instruments*, vol. 14, 2019, pp. 161–166.

[9] F. Aulia, M. Rif'an, and R. A. Setyawan, "Implementasi low pass filter digital IIR Butterworth pada FPGA," *Jurnal Mahasiswa Teknik Elektro Universitas Brawijaya*, vol. 1, no. 4, 2013.

[10] K. Gaikwad and M. Chavan, "Design and implementation of digital Butterworth IIR filter using xilinx system generator for noise reduction in ECG signal," *WSEAS Transactions on Electronics*, vol. 8, pp. 8–12, 2017.

[11] S. Roy, "Parallel and pipeline implementations of IIR low pass filter on FPGA," 2020.

[12] S. S. Pujari, P. P. Muduli, A. Panda, R. Badhai, S. Nayak, and Y. Sahoo, "Design and implementation of FIR filters using on-board ADC-DAC and FPGA," in *International Conference on Information Communication and Embedded Systems (ICICES2014)*, 2014, pp. 1–6.

[13] U. Meyer-Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, 4th ed. Berlin, Heidelberg: Springer, 2014.

[14] P. Virtanen *et al.*, "Scipy 1.0: Fundamental algorithms for scientific computing in python," *Nature Methods*, vol. 17, no. 3, pp. 261–272, 2020.

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[15] P. P. Chu, *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*. John Wiley & Sons, 2008.

[16] Xilinx Inc., *7 Series DSP48E1 Slice User Guide*, 2023, uG479.

[17] ——, *Vivado Design Suite User Guide: Design Analysis and Closure Techniques*, 2022, uG906.

[18] ——, *Vivado Design Suite User Guide: Power Analysis and Optimization*, 2021, uG907.