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Design and Analysis of a Low-Power 45 nm CMOS LNA for 2.4 GHz BLE Receivers Using Inductive Degeneration and PCSNIM Technique
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Universitas Gadjah Mada, 2026 | Diunduh dari http://etd.repository.ugm.ac.id/

INTISARI

Penerima *Bluetooth Low Energy* (BLE) membutuhkan penguat *front-end* berdaya rendah dengan *noise figure* minimum untuk mencapai sensitivitas yang memadai. Penelitian ini memaparkan perancangan dan analisis *Low Noise Amplifier* (LNA) CMOS 2,4 GHz berdaya rendah untuk aplikasi penerima BLE dengan menggunakan teknologi CMOS 45 nm gpdk045. Teknik *Power-Constrained Simultaneous Noise and Input Matching* (PCSNIM) diterapkan pada topologi kaskode dengan *inductive source degeneration* untuk mencapai *noise and impedance matching* secara bersamaan dengan batasan daya tertentu. Proses desain diawali dengan simulasi *parametric sweep* untuk menentukan nilai komponen awal, dilanjutkan dengan *tuning* iteratif pada tingkat skematik. Analisis non-idealitas dilakukan secara sistematis untuk mengidentifikasi penyebab utama penurunan kinerja saat beralih dari komponen ideal ke riil. Hasilnya menunjukkan bahwa induktor gerbang (L_g) merupakan penyumbang degradasi terbesar akibat rugi-rugi resistif pada induktor spiral *on-chip* yang berukuran besar.

Simulasi *post-layout* yang menggunakan *parasitic-extracted netlist* menghasilkan *noise figure* 2,97 dB, *input return loss* -30,19 dB, *gain* 17,99 dB, dan konsumsi daya 2,1 mW dengan tegangan catu 1 V. Seluruh hasil tersebut telah memenuhi spesifikasi target BLE dan membuktikan bahwa teknik PCSNIM sangat layak diterapkan untuk desain LNA berdaya rendah pada teknologi CMOS 45 nm.

Kata kunci: *Low Noise Amplifier (LNA), PCSNIM, Bluetooth Low Energy (BLE), CMOS, 45 nm, Noise Figure, Inductive Source Degeneration*

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ABSTRACT

Bluetooth Low Energy (BLE) receivers require low-power front-end amplifiers with minimal noise figure to achieve adequate receiver sensitivity. This research presents the design and analysis of a 2.4 GHz low-power CMOS Low Noise Amplifier (LNA) for BLE receiver applications, implemented in the gpdk045 45 nm CMOS technology. The Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) technique is applied to a cascode topology with inductive source degeneration to achieve near-simultaneous noise and impedance matching under a constrained power budget. The design process employs sequential parametric sweep simulations to establish preliminary component values, followed by iterative tuning at the schematic level. A systematic non-ideality analysis is conducted to identify the dominant source of performance degradation when transitioning from ideal to real components, revealing that the gate inductor L_g is the primary contributor due to resistive losses in large on-chip spiral inductors.

Post-layout simulation using a parasitic-extracted netlist yields a noise figure of 2.97 dB, an input return loss of -30.19 dB, an LNA gain of 17.99 dB, and a power consumption of 2.1 mW from a 1 V supply, all meeting the BLE target specifications. The results validate the applicability of the PCSNIM technique for low-power LNA design in 45 nm CMOS technology.

Keywords: *Low Noise Amplifier (LNA), PCSNIM, Bluetooth Low Energy (BLE), CMOS, 45 nm, Noise Figure, Inductive Source Degeneration*