

ENDORSEMENT PAGE	ii
STATEMENT	iii
PREFACE	iv
CONTENTS	v
LIST OF TABLES.....	vii
LIST OF FIGURES	viii
NOMENCLATURE AND ABBREVIATION	ix
ABSTRACT	x
INTISARI.....	xi
CHAPTER I INTRODUCTION	1
1.1 Background	1
1.2 Problem Formulation	2
1.3 Research Objectives	2
1.4 Research Limitations	2
1.5 Research Benefits	3
1.6 Writing Systematics	4
CHAPTER II LITERATURE REVIEW AND THEORETICAL BASIS	6
2.1 Literature Review	6
2.2 Theoretical Basis	7
2.2.1 Overview of Greatest Common Divisor (GCD)	7
2.2.2 Euclidean Algorithm	8
2.2.3 Hardware Implementation of Greatest Common Divisor (GCD)...	8
2.2.4 AMD Field-Programmable Gate Arrays (FPGAs)	9
2.2.5 MicroBlaze V Soft-Core Processor	9
2.2.6 AXI4-Lite Bus Protocol	10
2.2.7 Vivado Design Suite	12
CHAPTER III Research Methodology	14
3.1 Research Workflow	14
3.1.1 Phase 1: Processor and UART Test	14
3.1.2 Phase 2: AXI4-Lite Read/Write Transaction Test with Custom Module.....	15
3.1.2.1 Adder Module Design	16
3.1.2.2 AXI4-Lite Read Transaction	17
3.1.2.3 AXI4-Lite write Transaction	17
3.1.2.4 Adder Module Test	18
3.1.3 Phase 3: Greatest Common Divisor (GCD) Hardware Accelerator	18

3.1.3.1	Module Ports	21
3.1.3.2	Module Internal Registers	22
3.1.3.3	Module Local Parameters and States	22
3.1.3.4	Greatest Common Divisor (GCD) Module Pipelined Architecture	23
3.1.3.5	Memory Mapping and AXI4-Lite Interface	26
3.1.3.6	Software Application for GCD Hardware Accelerator ..	28
3.1.4	Phase 4: Greatest Common Divisor Benchmark	30
3.1.4.1	software Baseline	31
3.1.4.2	Hardware Accelerator Benchmark	33
3.2	Tools for the Research	34
3.3	Methods Used	35
3.3.1	Resource Utilization	35
3.3.2	Execution Time and Resource Utilization Ratio.....	36
CHAPTER IV RESULTS AND DISCUSSION		37
4.1	Processor and UART Test Results	37
4.2	AXI4-Lite Read/Write Transaction Test with Custom Module Result	38
4.3	Greatest Common Divisor (GCD) Hardware Accelerator Result	39
4.4	Final Benchmark Results	40
4.4.1	Execution Time Comparison	40
4.4.2	Resource Utilization Comparison	42
4.5	Execution Time and Resource Utilization Ratio Calculation	43
CHAPTER V Conclusion		48
REFERENCES		49
LAMPIRAN		L-1
L.1	Revision History	L-1
L.2	Read State Machine	L-1
L.3	Read Memory Mapped register Logic	L-3
L.4	Write State Machine	L-3
L.5	Write Memory Mapped register Logic.....	L-5
L.6	Adder C Code	L-7
L.7	Verilog Core: GCD for 12 digits	L-8
L.8	Serial Result of 2 - 12 Numbers GCD Calculation	L-15
L.9	AXI4-Lite Timing Diagram	L-18