

TABLE OF CONTENTS

PREFACE.....	i
TABLE OF CONTENTS	iii
LIST OF FIGURES	vi
LIST OF TABLES	viii
INTISARI.....	ix
ABSTRACT	x
CHAPTER I INTRODUCTION	12
1.1 Background.....	12
1.2 Problem Statement.....	14
1.3 Problem Limitations	14
1.4 Purpose of Research	14
1.5 Benefit of Research	14
1.6 Research Methodology	15
1.7 Systematic of Writing.....	16
CHAPTER II LITERATURE REVIEW	17
2.1. Hardware Design Considerations in FPGA.....	17
2.2. Effective Data Transfer	18
2.3. Open Source Tools and Firmware.....	19
CHAPTER III THEORETICAL FOUNDATION	24
3.1 DHT11 Sensor	24
3.1.1 DHT11 Communication Protocol.....	25
3.1.2 Temperature.....	26
3.1.3 Humidity.....	26
3.2 Field Programmable Gate Array (FPGA).....	27
3.2.1 <i>Open-Source</i>	28
3.2.2 <i>Lattice iCE40</i>	29
3.3 Verilog.....	31
3.4 Yosys	32
3.5 Nextpnr	34



3.6 Microcontroller.....	36
3.6.1 ESP32	37
3.7 MQTT.....	38
CHAPTER IV RESEARCH METHODOLOGY	42
4.1 Research Procedures.....	42
4.2 Tools and Materials	43
4.3 System Design	44
4.3.1 Hardware Architecture Design	44
4.3.2 Sensor Data Acquisition System Development.....	47
4.3.3 MQTT Wireless Communication Protocol Development.....	49
4.3.4 Open-source EDA System Development	51
4.4 System Testing	52
4.4.1 Component Testing	52
4.4.2 Communication Testing	53
4.4.3 Overall System Testing	53
CHAPTER V IMPLEMENTATION	54
5.1 Hardware Implementation	54
5.2 System Array	55
5.3 DHT11 Interface Module	56
5.4 UART Module.....	59
5.5 Top Module	61
5.6 Physical Constraint File.....	63
5.7 Testbench Implementation	64
5.8 APIO Tool-Chain Utilization	66
5.9 ESP32 UART Receiver and IoT Capabilities Implementation	69
5.10 DHT11 Data Acquisition and Telemetry Finalization	72
CHAPTER VI RESULTS AND DISCUSSION	75
6.1 System Performance and Parallel Data Acquisition Result.....	75
6.1.1 Parallel Data Acquisition Timing Benchmark	75
6.1.2 Parallel Data Acquisition Findings.....	77
6.2 UART Data Transmission	79



6.2.1 Total Accumulated Time from Data Acquisition to UART Output.....	80
6.2.2 UART Data Precision Result.....	81
6.2.3 UART Data Findings.....	81
6.3 MQTT Dashboard Result	82
6.3.1 Received Payload Precision.....	82
6.4 Resource Utilization Results	84
6.4.1 Yosys Synthesis Utilization.....	84
6.4.2 Physical Device Utilization	86
6.4.3 System Timing.....	87
6.4.4 Hardware Development Findings.....	87
CHAPTER VII CONCLUSION.....	89
7.1 Conclusion.....	89
7.2 Recommendation	90

LIST OF FIGURES

Figure 3.1 DHT11 Sensor.....	24
Figure 3.2 DHT11 Communication Process (Umang Gajera, 2017)	26
Figure 3.3 Birds-eye view of FPGA and its components (Lattice Semiconductor, n.d.).....	28
Figure 3.4 Digital design flow based on APIO (Navarro-Torrero et al., 2024)	29
Figure 3.5 Lattice iCE40 FPGA Block Diagram (Lattice Semiconductor, n.d.)....	30
Figure 3.6 Example String Manipulation Code in VHDL (IEEE Behavioural languages - Part 4: Verilog hardware description language, 2001).....	32
Figure 3.7 Simple RTL Netlist Synthesized Via Yosys (Yosyshq, n.d)	33
Figure 3.8 Yosys synthesis recursive (Shah et al., 2019).....	34
Figure 3.9 Nextpnr GUI (Shah et al., 2019)	35
Figure 3.10 Microcontroller Architecture (Y Shi, 2020).....	37
Figure 3.11 ESP32 Block Scheme (Babiuch et al., 2019).....	38
Figure 3.12 Publisher/subscriber flow diagram (Yassein & Shatnawi, 2017)	39
Figure 3.13 Thingsboard Cloud Broker Dashboard	40
Figure 4.1 Research Flow Diagram.....	42
Figure 4.2 General System Design.....	44
Figure 4.3 Function Diagram.....	44
Figure 4.4 Hardware Components.....	45
Figure 4.5 Architecture Design	46
Figure 4.6 Acquisition Module.....	48
Figure 4.7 Transmission FPGA Design.....	49
Figure 5.1 Hardware Implementation.....	54
Figure 5.2 PCB Schematic.....	55
Figure 5.3 System Array.....	55
Figure 5.4 SB_IO Primitive DHT11 Interfacing Module	57
Figure 5.5 Timing Parameters DHT11 Interfacing Module	58
Figure 5.6 DHT11 Interface Module FSM.....	59

Figure 5.7 Excerpt of UART Module.....	60
Figure 5.8 Excerpt of Top Module	61
Figure 5.9 Top Module FSM.....	62
Figure 5.10 FPGA PMOD Connector Pin Utilization.....	63
Figure 5.11 Top Module PCF.....	63
Figure 5.12 UART Module Testbench	65
Figure 5.13 APIO Design Flow	66
Figure 5.14 GTK Wave Dashboard.....	66
Figure 5.15 Apio Sim Operator	67
Figure 5.16 Apio Build Operator.....	67
Figure 5.17 Top Module Yosys Component Usage	68
Figure 5.18 Top Module NextPNR Device Utilization.....	68
Figure 5.19 Apio Upload Operator.....	69
Figure 5.20 ESP32 UART Receiver and MQTT Payload Transmitter	71
Figure 5.21 Device MQTT Dashboard Connection Verification	72
Figure 5.22 Saleae Logic Analyzer DHT11 Input and UART Output.....	72
Figure 5.23 Local and Remote Telemetry	73
Figure 5.24 Thingsboard Telemetry	74
Figure 6.1 DHT11 Handshake Time Taken	76
Figure 6.2 DHT11 Sampled Data Benchmark.....	76
Figure 6.3 DHT11 Data Line.....	77
Figure 6.4 Verilog Ternary Hi-Z Operator.....	78
Figure 6.5 Yosys Limited Tri-State Hi-Z Logic Error Message	79
Figure 6.6 SB_IO Primitive Block	79
Figure 6.7 Total Accumulated Time.....	80
Figure 6.8 Payload Verification.....	83
Figure 6.9 Dashboard Precision With Payload and Efficiency	84
Figure 6.10 Yosys Top Level Device Utilization.....	85
Figure 6.11 Nextpnr Mapped Device Utilization Compiler Report	86
Figure 6.12 System Timing Analysis	87
Figure 6.13 6 DHT11 Sensor Interface LC Usage	88



Figure 6.14 LC Exceed Limit Error Compilation Message..... 88

LIST OF TABLES

Tabel 2.1 Research Correlation	20
Tabel 2.2 Research Correlation (Continuation).....	21
Tabel 2.3 Research Correlation (Continuation).....	22
Tabel 2.4 Research Correlation (Continuation).....	23
Tabel 4.1 List of Tools	43
Tabel 4.2 List of Materials	44
Tabel 6.1 DHT11 Datasheet Timing Constraints vs Hardware Timing Constraints	78
Tabel 6.2 UART Data Precision.....	81
Tabel 6.3 Payload Precision	83
Tabel 6.4 Nextpnr Mapped Device Utilization	86