DAFTAR PUSTAKA

Abdulazeez, A. M., & Tahir, A. S. (2013, September). Design and Implementation of Advanced Encryption Standard Security Algorithm using FPGA. *International Journal of Scientific & Engineering Research*, *4*(9), 1988-1993.

Afianah, N., Putra, A. E., & Dharmawan, A. (2019). High-Level Synthesize of Backpropagation Artificial Neural Network Algorithm on the FPGA. *2019 5th International Conference on Science and Technology (ICST), Yogyakarta, Indonesia*, 1-5.

Alsuwaiyan, A., Habib, A. A., Imoukhuede, A. B., Omar, M. O., Maruf, M. A., Alqarni, M., El-Maleh, A., Tabbakh, A., Felemban, M., & Azim, A. (2024). A Systematic Literature Review on Vulnerabilities, Mitigation Techniques, and Attacks in Field-Programmable Gate Arrays. *Arabian Journal for Science and Engineering*, *50*(1), 611-641.

Atteya, A. M., & Madian, A. M. (2014). Hybrid Chaos-AES Encryption Algorithm and Its Implementation Based on FPGA. *014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), Trois-Rivieres, QC, Canada*, 217-220.

Augoestien, N. G., & Putra, A. E. (2015, Oktober). Purwarupa Perangkat Keras untuk Eksekusi Algoritma AES Berbasis FPGA. *IJEIS*, *5*(No. 2), 211-220.

Canis,, A., Anderson, J. H., & Brown, S. D. (2013). Multi-Pumping for Resource Reduction in FPGA High-Level Synthesis. *013 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France*, 194-197.

Daoud, L., Hussein, F., & Rafla, N. (2019). Optimization of Advanced Encryption Standard (AES) Using Vivado High Level Synthesis (HLS). *Proceedings of 34th International Conference on Computers and Their Applications*, *58*, 36-44.

Digilent. (2016). Arty 7. *https://digilent.com/reference/programmable-logic/arty-a7/start?srsltid=AfmBOopYWjXM2CPkJk-Qz9wfaLGVwa9kGErt6JqhwE4i475nfRwEpSLr*. Diakses tanggal 5 Desember 2024.

Georgiou, G., & Theodoridis, G. (2021). Studying the impacts of loop unrolling and pipeline in the FPGA design of the Simon and RoadRunneR lightweight ciphers. *2021 10th International Conference on Modern Circuits and Systems Technologies (MOCAST), Thessaloniki, Greece*, 1-6.

Good, T., & Benaissa, M. (2005). AES on FPGA from the Fastest to the Smallest. *In J. R. Rao & B. Sunar (Eds.), Cryptographic Hardware and Embedded Systems - CHES*, 427-440.

Grycel, J. T., & Walls, R. J. (2019). DRAB-LOCUS: An Area-Efficient AES Architecture for Hardware Accelerator Co-Location on FPGAs. *2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain*, 1-5.

Hadjis, S., Canis, A., Anderson, J., Choi, J., Nam, K., Brown, S., & Czajkowski, T. (2012). Impact of FPGA Architecture on Resource Sharing in High-Level Synthesis. *Proceedings of the ACM/SIGDA 20th International Symposium on Field Programmable Gate Array*, 111-114.

Hakim, Z., Natan, O., Sari, R. H., Amael, J. T., Dharmawan, A., & Istiyanto, J. E. (2024). 6-DOF Arm Robot Control Using Open-Source FPGA. *2024 9th International Conference on Control and Robotics Engineering, Osaka, Japan*, 157-161

Harb, S., Ahmad, M. O., & Swamy, M.N. S. (2022). A High-Speed FPGA Implementation of AES for Large Scale Embedded Systems and its Applications. *2022 13th International Conference on Information and Communication Systems (ICICS), Irbid, Jordan*, 59-64.

Ibrahimov, B. G., Humbatov, R. T., & Ibrahimov, R. F. (2018). Information in Telecommunication Systems. *IFAC (International Federation of Automatic Control)*, 821-824

Irfan1,, M., & Setiawan, H. (2022, Desember). IMPLEMENTASI KOMPUTASI AKAR KUADRAT RESOLUSI TINGGI PADA FIELD PROGRAMMABLE GATE ARRAY (FPGA). *Jurnal Teknologi Informasi dan Ilmu Komputer (JTIIK)*, *9*(7), 1617-1622.

Jatmiko, W., Mursanto, P., Fajar, M., Tawakal, M. I., Trianggoro, W., Rambe, R. S., Fauzi, & Ramadhan, A. (2011). *IMPLEMENTASI BERBAGAI ALGORITMA NEURAL NETWORK DAN WAVELET PADA FIELD PROGRAMMABLE GATE ARRAY (FPGA)* (1st ed.). Perpustakaan Nasional: Katalog Dalam Terbitan.

Lee, U., Kim, H. K., Lim, Y. J., & Sunwoo, M. H. (n.d.). Resource-Efficient FPGA Implementation of Advanced Encryption Standard. *2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX*, 1165-1169.

Maxfield, C. (2004). *The design warrior's guide to FPGAs: devices, tools, and flows*. Elsevier Science. United States of America.

NLnet Foundation. (2024). *FPGA Fault Injection Testing*. nlnetfoundation. Diakses 7 Maret 2025, dari https://nlnet.nl/project/FPGA-Inject/.

Pailler, P. (1999). Evaluating Differential Fault Analysis of Unknown Cryptosystems. In: Public Key Cryptography. *PKC 1999. Lecture Notes in Computer Science*, *1560*.

Purohit, S., Deshpande, V., & Ingale, D. V. (2023). FPGA Implementation of the AES Algorithm with Lightweight LFSR-Based Approach and Optimized Key Expansion. *2023 IEEE International Conference on Public Key Infrastructure and its Applications (PKIA), Bangalore, India*, 1-7.

Qadir, A. M., & Varol, N. (2019). A Review Paper on Cryptography. *2019 7th International Symposium on Digital Forensics and Security (ISDFS)*. 1-6.

Rahimunnisa, K., Karthigaikumar, P., Rasheed, S., Jayakumar, J., & Kumar, S. S. (2012, Oktober 12). FPGA implementation of AES algorithm for high throughput using folded parallel architecture. *SECURITY AND COMMUNICATION NETWORKS*, (7), 2225-2236.

Rusdi, M., Samman, F. A., Sadjad, R. S., Salam, A. E. U., & Machbub, C. (2020). Standalone Single Phase DC-AC Inverter with FPGA-based Pulse Modulated Generator Unit. *2020 International Seminar on Intelligent Technology and Its Applications (ISITIA), Surabaya, Indonesia*, 7-12.

Shahbazi, K., & Ko, S.-B. (2020, September 10). High throughput and area-efficient FPGA implementation of AES for high-traffic applications. *IET Computers & Digital Techniques*, *14*(6), 344-352.

Smoliński, Ł., Barkalov, A., & Titarenko, L. (2014, Desember). The Application and Adaptation of the Two Sources of Code and Natural Encoding Method for Designing a Model of Microprogram Control Unit with Base Structure. *Circuits and Systems*, *5*, 301-308.

Sunil1,, J., S, S. H., K, S. B., & Santhameena4, S. (2020, November). Implementation of AES Algorithm on FPGA and on software. *2020 IEEE International Conference for Innovation in Technology (INOCON), Bengaluru, India*, 1-4.

Ueno, R., Marioka, S., Miura, N., Matsuda, K., Nagata, M., Bhasin, S., Mathieu, Y., Graba, T., Danger, J.-L., & Homma, N. (2020, April 4). High

Throughput/Gate AES Hardware Architectures Based on Datapath Compression. *IEEE TRANSACTIONS ON COMPUTERS*, *69*(4), 534-548.

Widianto, M. H. (2019). *Teknologi pada FPGA(Field Programmable Gate Array)*. Binus.ac.id. *https://binus.ac.id/bandung/2019/12/teknologi-pada-fpga-field-programmable-gate-array*. Diakses tanggal 4 Desember 2024.

Xilinx. (2020). *https://digilent.com/reference/programmable-logic/nexys-4/start?srsltid=AfmBOoqVbKocTIW6MyQrL7e_5oRbbAzsNJK4vFtKAOrCq9Wo0vrqOzSU*. Diakses tanggal 4 Desember 2024.

Yadav, S., Girdhar, G., & Vinitha, C. (2024). AES 128 BIT OPTIMIZATION: HIGH SPEED AND AREA-EFFICIENT THROUGH LOOP UNROLLING. *2024 IEEE Region 10 Symposium (TENSYMP), New Delhi, India*, 1-8.

Yadav, V. K., Singh, S., & Sharma, D. G. (2022). A Review of Cryptography Techniques for Securing Data on Messaging and Cloud Applications. *2022 4th International Conference on Advances in Computing, Communication Control and Networking (ICAC3N), Greater Noida, India*, 1880-1884.

Zakirman, W. A. (2020). Implementasi Aritmatika Modular Pada Field Programmable Gate Array (FPGA) Menggunakan Algoritma ALDMAS. *Skripsi*, Fakultas MIPA, Universitas Gadjah Mada, Yogyakarta.