DAFTAR PUSTAKA

Anitha, K., Kumar Gopathoti, K., Rajeswari, J., Majji, S., Radhika Patnala, T., & Sri Sai Satyanarayana, D. (2021). FPGA Implementation of Arbiter PUFs for ideal Cryptographic Key Generation. *Proceedings of the 5th International Conference on Electronics, Communication and Aerospace Technology, ICECA 2021*, *Iceca*, 754–757.

Aravindan, M., & Kokila, J. (2022). Practical Challenges in Simulating Strong PUFs. *2022 IEEE IAS Global Conference on Emerging Technologies, GlobConET 2022*, 471–476.

Arthur, S., & Doyle, C. (n.d.). *Pipelining : Basic and*.

Chu, P. P. (2011). FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version. In *FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version*.

Fan, H., Ferianc, M., Que, Z., Liu, S., Niu, X., Rodrigues, M. R. D., & Luk, W. (2022). FPGA-Based Acceleration for Bayesian Convolutional Neural Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *41*(12), 5343–5356.

Flash, S. (2016). *Nexys 4^{TM} FPGA Board Reference Manual*. 1–29.

Gehrer, S. (2017). *Highly Efficient Implementation of Physical Unclonable Functions on FPGAs*. *August*.

Gireesh, A., Bhakthavatchalu, R., & Devika, K. N. (2022). Performance Analysis of Different Types of Delay based PUFs. *2022 6th International Conference on Trends in Electronics and Informatics, ICOEI 2022 - Proceedings*, *Icoei*, 180–184.

Hatti, K., & Paramasivam, C. (2021). The MUX-Based PUF Architecture for Hardware Security. *2021 International Conference on Circuits, Controls and Communications, CCUBE 2021*, 1–7.

Iverson, B. L., & Dervan, P. B. (n.d.). *Physical Unclonable Functions in Theory and Practice*.

Jatmiko, W. (2011). *Implementasi Berbagai Algoritma Neural Network Dan Wavelet Pada Field Programmable Gate Array* (Nomor August 2016).

Khanam, J., & Cavicchi, K. A. (2023). Design and Implementation of a Strong Arbiter PUF for the Security of FPGA. *2023 IEEE 14th Annual Ubiquitous Computing, Electronics and Mobile Communication Conference, UEMCON 2023*, 674–677.

Kulkarni, S., Vani, R. M., & Hunagund, P. V. (2021). *Designing of Arbiter PUF for Securing IP and IoT Devices*. *January*, 131–138.

Kurra, A. K., & Nelakuditi, U. R. (2019). *A secure arbiter physical unclonable functions (PUFs) for device authentication and identification*. *7*(1), 117–127.

Mahalat, M. H., Mandal, S., Mondal, A., & Sen, B. (n.d.). *An Efficient Implementation of Arbiter PUF on FPGA for IoT Application*. 324–329.

Sumayyabeevi, V. A., Poovely, J. J., Aswathy, N., & Chinnu, S. (2021). A New Hardware Architecture for FPGA Implementation of Feed Forward Neural Networks. *ACCESS 2021 - Proceedings of 2021 2nd International Conference on Advances in Computing, Communication, Embedded and Secure Systems*, *September*, 107–111.

Yao, S., & Zhang, L. (2022). FHAM: FPGA-based High-Efficiency Approximate Multipliers via LUT Encoding. *Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors*, *2022-Octob*(Iccd), 487–490.